CLAIM LISTING:

1-11. (Cancelled)

12. (New) A circuit comprising:

a processor; and

a memory connected to the processor, said memory storing a plurality of instructions, wherein execution of the instructions by the processor causes:

(a) generating a sequence of binary addresses with a length N, wherein N is greater or equal to a desired sequence length D, wherein N is a power of 2;

(b) selecting a combination of D addresses from the generated sequence;

(c) checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses; and

(d) repeating (b) and (c) until a combination of D addresses that satisfies the one bit difference property is found.

13. (New) The circuit according to claim 12 wherein the length D is an odd number.

14. (New) The circuit according to claim 12 wherein D is the depth of a data structure.

15. (New) A method for generating a sequence of binary addresses of length D, the method comprising:

(a) generating a sequence of binary addresses with a length N, wherein N is greater or equal to the desired sequence length D, wherein N is a power of 2;

(b) selecting a combination of D addresses from the generated sequence;

(c) checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses; and

(d) repeating (b) and (c) until a combination of D addresses that satisfies the one bit difference property is found.

16. (New) The method according to claim 15 wherein the length D is an odd number.

17. (New) The method according to claim 15 wherein D is the depth of a data structure.